LISTING OF THE CLAIMS

CLAIMS

We claim:

1. (Currently amended) An apparatus comprising:

a descriptor table - said apparatus for controlling flow of data between first and second data processing systems via a memory, said descriptor table for storing a plurality of descriptors for access by the first and second data processing systems, said first processing system comprises a plurality of host computer systems, said second data processing comprising a plurality of attached devices interconnected by an intervening network architecture, said network architecture comprises a plurality of data communications switches, said host computer system and the attached devices each forming a node in a data processing network, each host computer system comprising a plurality of central processing units and a memory interconnected by a PCI bus architecture;

a network adapter also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture; and

descriptor logic for generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table,

wherein:

the network adapter comprises a pluggable option card having a connector such as an edge connector for removable insertion into the bus architecture of the host computer system, said option card carrying:

an Integrated System on a Chip connected to the bus architecture via a connector,

at least one third level memory modules connected to the chip, and

an interposer connected to the chip for communicating data between media of the network architecture and the chip, said interposer providing a physical connection to the network, and,

wherein the descriptors generated by the descriptor logic comprise a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory;

wherein the memory is implemented by a combination of SRAM and SDRAM, said chip including a memory subsystem of the adapter comprises a first and a second memory, a data cache and an instruction cache associated with a TX processor, and a second data cache and second instruction cache associated with an RX processor, said three levels of memory having respective sizes and associated access times, such that the memory subsystem facilitates: convenient access to instruction and data by both the TX processor and the RX processor; scaleability; and sharing of resources between the TX processor and the RX processor in the interests of reducing manufacturing costs, and

wherein the descriptor table is stored in the memory of the first data processing system.

2. - 3. (Canceled)

4. (Previously presented) An apparatus as claimed in claim 1 ~~claim 3~~, further permitting coexistence of heterogeneous communication protocols between the adapters and the host systems serving various applications, such that use the adapter and a predefined set of data structures enhancing data transfers between the host and the adapter, and opening a number of application channels that can be opened in parallel as determined by an amount of memory

resources allocated to the adapter and being independent of processing power embedded in the adapter, and

wherein the descriptor table is stored in a memory of the second data processing system.

5. (Previously presented) An apparatus as claimed in claim 1 ~~claim 3~~ ,

wherein a branch descriptor comprises description of the descriptor location being link lists of descriptors,

wherein information in the descriptors is used for control by software in the host of data movement operations performed by TX and RX LCP engines, said information being used to process a frame to generate a TX packet header located in the header of the frame, and

wherein the descriptor table comprises a plurality of descriptor lists sequentially linked together via branch descriptors therein.

6. (original) An apparatus as claimed in claim 1, wherein the descriptor table comprises a cyclic descriptor list.

7. (original) An apparatus as claimed in claim 1, wherein the first data processing system comprises a host computer system.

8. (Previously presented) An apparatus as claimed in claim 1, wherein the second data processing system comprises a data communications interface for communicating data between a host computer system and a data communications network.

9. (previously presented) A data processing system comprising: a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, and apparatus as claimed in claim 1, for controlling

flow of data between the memory of the host computer system and the data communications interface

10. (Previously presented) A method comprising:

controlling flow of data between first and second data processing systems via a memory, the step of controlling comprising: storing in a descriptor table a plurality of descriptors for access by the first and second data processing systems,

forming said first processing system to comprise a plurality of host computer systems, said second data processing to comprise a plurality of attached devices interconnected by an intervening network architecture, said network architecture comprising a plurality of data communications switches, said host computer system and the attached devices each forming a node in a data processing network, each host computer system comprising a plurality of central processing units and a memory interconnected by a PCI bus architecture;

including a network adapter also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture; and

by descriptor logic, generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table.

. 11. (Currently amended) A method as claimed in claim 10, further comprising,

implementing the network adapter to comprise a pluggable option card having a connector such as an edge connector for removable insertion into the bus architecture of the host computer system, said option card carrying:

an Integrated System on a Chip connected to the bus architecture via a connector,

at least one third level memory modules connected to the chip, and

an interposer connected to the chip for communicating data between media of the network architecture and the chip, said interposer providing a physical connection to the network, and advantageously reducing manufacturing costs and providing reusable system building blocks,

and,

by the descriptor logic, generating a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory, and further comprising:
implementing the memory by a combination of SRAM and SDRAM, said chip including a memory subsystem of the adapter comprises a first and a second memory, a data cache and an instruction cache associated with a TX processor, and a second data cache and second instruction cache associated with an RX processor, said three levels of memory having respective sizes and associated access times, such that the memory subsystem facilitates: convenient access to instruction and data by both the TX processor and the RX processor; scaleability; and sharing of resources between the TX processor and the RX processor in the interests of reducing manufacturing costs, and
storing the descriptor table in the memory of the first data processing system.

12. (Canceled)

13. (Currently amended) A method as claimed in claim 11 ~~claim 12~~, further comprising permitting coexistence of heterogeneous communication protocols between adapters and the host system serving various applications, such that use the adapter and a predefined set of data structures enhancing data transfers between the host and the adapter;

opening a number of application channels in parallel as determined by an amount of memory resources allocated to the adapter and being independent of processing power embedded in the adapter. It will be appreciated from the following that the ISOC 120 concept of integrating multiple components into a single integrated circuit chip component advantageously minimizes manufacturing costs and in provides reusable system building blocks. However, it will also be appreciated that in other embodiments of the present invention, the elements of the ISOC 120 may be implemented by discrete components, and

storing the descriptor table in a memory of the second data processing system.

14. (Previously presented) A method as claimed in claim 10, comprising forming the descriptor table by linking a plurality of descriptor lists in series via branch descriptors therein, wherein a branch descriptor comprises description of the descriptor location being link lists of descriptors,

using information in the descriptors for control by software in the host of data movement operations performed by TX and RX LCP engines,

using the information to process a frame to generate a TX packet header in the header of the frame.

15. (original) A method as claimed in claim 10, wherein the first data processing system comprises a host computer system.

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16. (Previously presented) A method as claimed in claim 10, wherein the second data processing system comprises a data communications interface for communicating data between a host computer system and a data communications network.

17. (original) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing control of flow of data between first and second data processing systems, the computer readable program code means in

said computer program product comprising computer readable program code means for causing a computer to effect the functions of claim 1.

18. (original) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing data processing, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect the functions of claim 9.

19. (original) An article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing control of flow of data between first and second data processing systems, the computer readable program code means in said article of manufacture comprising computer readable program code means for causing a computer to effect the steps of claim 10.

20. (original) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for controlling flow of data between first and second data processing systems, said method steps comprising the steps of claim 10.

21. (previously presented) An apparatus as claimed in claim 1, wherein:

the descriptors generated by the descriptor logic comprise a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory;

the descriptor table is stored in one of the memory of the first data processing system and the second data processing system;

the descriptor table comprises a plurality of descriptor lists sequentially linked together via branch descriptors therein;

the descriptor table comprises a cyclic descriptor list;

the first data processing system comprises a host computer system; and

the second data processing system comprises a data communications interface for communicating data between a host computer system and a data communications network..